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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,917	12/16/2003	Yoshihiro Koga	60188-732	3835

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EXAMINER	
VO, THANH DUC	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,917	KOGA ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4, 5, 7, 8, 10, 11, 13, 14, 16, 17, 18, 20, 21, 23, 24, 26, 27, 29, 30, 32, 33, 36, 37, 39, 40, and 42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claims 4, 17, and 30, they are indefinite since they are not particularly point out if "reads data from the requested address **in** the released page memory unit" or **into** or **from** the released page memory unit.

As to remainder of above claims, the sentence structure of each and every claim is not clearly pointed out the subject matter of the claim invention. For example, claim 5 is written:

"wherein the replacement control unit evenly redistributes, when an application program to be executed is changed, empty memories to application programs under operation."

The claiming subject matter is not cleared whether "the replacement control unit evenly redistributes when an application program to be executed is change, then empty memories to application program under operation" or "the replacement control unit evenly redistributes; when an application program to be executed is change, empty memories to application program under operation". In addition, it is not clear on how

"the replacement control unit evenly redistributes" and what are there that are being evenly redistributed.

The structural relationship of the claim invention is also not correlated and containing disconnected relationship therefore they are indefinite.

The applicant is required to make appropriate corrections in the respective paragraphs corresponded or related to above claims in the specification including the Summary and Detailed Specification since the claim language is directly copied from the specifications.

In addition, applicant is required to make clear to remainder of the rejected claims above which are vague and omitting the structural relationship in the claiming subject matters.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 17, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamizaki et al. (U.S. Patent 6,233,195) in view of Matick (U.S. Patent 4,084,230).

As to claim 1, Yamizaki et al. disclosed a semiconductor device comprising:

a processor (see col. 9, lines 5-13 and Fig. 40-CPU);

a first memory unit accessed by the processor (see col. 1, line 30, Fig. 4-DRAM);

a plurality of page memory units (see col. 8, lines 5-15) obtained by partitioning a second memory unit (see col. 1, lines 33-35, col. 8, lines 5-15, and Fig. 40-SCH) which is accessible by the processor at a speed higher than a speed at which the first memory unit is accessible;

a tag for adding, to each of the page memory units, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority (See col. 35, lines 37-57);

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag (See col. 35, line 37 – col. 36, line 44); and

Yamizaki et al. failed to disclose a replacement control unit for replacing respective contents of the page memory units.

Matick disclosed a replacement control unit for replacing respective contents of the page memory units. See col. 8, lines 27-37.

Yamizaki et al. and Matick are from the same field of endeavor, which is semiconductor memory and cache replacement algorithm.

At the time of applicant's invention it would have been obvious to one having ordinary skill in the art to modify the system of Yamizaki et al. to combine with the system of Matick to arrive at the invention in claim 1. The motivation of doing so is to

come up with a cache system that has a page replacement algorithm in order to replace and organize the cached contents so that the cache hit rate is higher, the memory access time is reduced and therefore, the processing efficiency will increase.

In addition, it would have been obvious to one having an ordinary skill in the computer art at the time of applicant's invention to implement a page memory unit having a larger storage capacity than a line in a cache memory since a larger page than a line will make the processing function and page replacement algorithm easier to design and manage by the operating system.

As to claim 2, Yamizaki et al. disclosed a semiconductor device further comprising: a distribution managing unit for managing the number of pages allocated to each of the page memory units for each function of an application program executed by the processor. See col. 7, lines 35-49.

As to claim 3, Yamizaki et al. disclosed semiconductor device wherein the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories, the semiconductor device further comprising: a bank control unit for managing the plurality of bank memories. See col. 7, line 63 – col. 8, line 4.

As to claims 4, 17, and 30, Yamizaki et al. disclosed a semiconductor device, wherein the replacement control unit determines whether or not information on a requested address of the page memory unit is held in the tag upon receipt of an access request to any of the page memory units (see col. 35, lines 38-50);

select one of the plurality of page memory units if the address information is not held in the tag based on preliminarily specified replacement information (see col. 35, lines 51-57, and col. 38, lines 16-22);

release the selected page memory unit and reads data from the requested address into the released page memory unit. See claim 2.

5. Claims 5-16, and 18-29, and 31-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamizaki et al. and Matick as applied to claim 1-4, 17, and 30 above, and further in view of Grunwald et al. (Published document: Improving the Cache Locality of Memory Allocation).

As to claims 5, 8, 11, 14, 18, 21, 24, 27, 31, 34, 37, and 40, Matick disclosed a page replacement algorithm wherein dependent on the priority. See col. 8, lines 8-35.

Grunwald et al. further disclosed a semiconductor device, wherein the replacement control unit evenly redistributes the empty memories to the individual applications in the event of an application change (see page 2, GNU Local);

Yamizaki et la., Matick, and Grunwald et al. are analogous art since they are from the same field of endeavor, which is cache replacement algorithm and memory allocation.

At the time of applicant's invention it would have been obvious to one having an ordinary skill in the art to realize that the method of Grunwald et al. is advantageous to implement to the system of Yamizaki et al. and Matick.

The motivation of doing so is to introduce a system that contains various replacement algorithms in order to allocate or distribute the memory to the program applications that are under operation so that all of the applications can run efficiently with an available amount of memory.

As to claims 6, 9, 12, 15, 19, 22, 25, 28, 32, 35, 38, and 41, Yamizaki et al. disclosed a semiconductor device wherein, upon receipt of a new memory reserve request, the replacement control unit selects and releases the one of the empty memories allocated to the application programs under operation which is in any of the page memory units or in any of the bank memories and has a small amount of information transferred between itself and the first memory unit. See col. 6, lines 27-62.

As to claims 7, 10, 13, 16, 20, 23, 26, 29, 33, 36, 39, and 42, Yamizaki et al disclosed the semiconductor device, wherein the replacement control unit performs reservation/activate and release/inactivate of the page memory units and brings the allocated empty memory into a releasable state. See col. 4, line 55 – col. 5, line 3; and col. 5, lines 30-40.

In addition, the program operation cycle is a well known method in the computer art to regulate all of the processes within a system in order to keep the system running flawlessly while increasing the system performance. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to realize and modify the clock of the system in order to arrive the invention in said claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanh D. Vo

Patent Examiner

01/23/2008

TUAN V. THAI
PRIMARY EXAMINER